REMARKS

Rejection of Claims 1-6 and 8-11 under 35 U.S.C. § 103(a)

The Examiner rejected Claims 1-6 and 8-11, under 35 U.S.C. § 103(a) as being unpatentable over Pan (US 5,595,919), in view of Wu (US 6,190,977 B1), stating that Pan discloses the method steps of:

providing a gate oxide and gate;

performing a source/drain extension implant (30, fig. 9);

forming spacer on the gate (22, fig. 3);

removing the spacer (fig. 7); and

performing a halo implant (34, fig. 11) (col. 2, ln. 59 - col. 3, ln. 54) and that Wu teaches the following limitations:

the gate defining a channel region of no more than 50 nm length (col. 1, lns. 54-76);

performing epitaxy to form raised source/drain regions (26, fig. 5); and

forming a silicide (32a,b, fig. 7) on the gate and source/drain regions (col. 5, lns. 50-56 and col. 6, lns.14-37).

Claims 1-6 and 8-11 are not herein further amended. The Applicant hereby respectfully traverses the Examiner's ground for rejection of Claims 1-6 and 8-11 on this basis. Pan specifically teaches that the source/drain extension implant (30) forms a "lightly doped source and drain region 30" (col. 3, ll. 41-42; Fig. 9). Pan's lightly doped source and drain regions 30 are created ***after*** removing the spacer, ***not before*** forming the spacer (col. 3, ll. 34-35), wherein "[t]he silicon nitride walls 22 are stripped." Further, Wu merely describes the need for "shorter channels," and does not teach any specific dimensions for any such shorter channels (col. 1, ll. 54-76). As such, the Applicant respectfully submits that Pan, even in view of Wu, does not teach, motivate, nor suggest the presently claimed 50-nm wide channels.

In contrast to Pan, even in view of Wu, the present method of Claim 1 comprises the sequential steps of:

providing a substrate having a gate oxide and gate thereon, the gate defining a channel region of no more than 50 nm length;

performing a source/drain extension implant;

forming a spacer on the gate;

performing epitaxy to form raised source/drain regions;

forming a silicide on the gate and source/drain regions;

removing the spacer;

performing a halo implant; and

completing the MOSFET.

The presently claimed step of "performing a source/drain extension implant" results in forming the presently claimed source/drain junctions 11. The source/drain junctions 11 are formed ***before*** the raised source/drain regions are formed, and as such, the source/drain junctions 11 extend from the isolation trenches 6 to the gate 3 (Fig. 1). In contrast, the lightly doped source and drain regions 30 of Pan are formed ***after*** the oxide layer 26 has been formed and ***after*** the spacer 22 has been removed. Resultantly, the lightly doped source and drain regions 30 extend between the oxide layer 26 and the gate 16 of Pan. As such, the Applicant respectfully submits that *the presently claimed forming of the source/drain junctions 11 could not be formed by the method disclosed by Pan, even in view of Wu.*

Further, Claim 5 of the present application comprises the steps of:

providing a substrate having a gate oxide and gate thereon, the gate defining a channel region of no more than 50 nm length;

performing a vertical source/drain extension implant to a depth of approximately 10 nm to approximately 30 nm;

forming a spacer on the gate;

forming raised source/drain regions;

forming a silicide on the gate and source/drain regions;

removing the spacer;

performing a halo implant; and

completing the MOSFET.

Claim 5 comprises the same sequence of relevant steps as recited in Claim 1. As such, the Applicant respectfully submits the same arguments advanced, supra, to the rejection of Claim 5. Specifically, the step of "performing a vertical source/drain extension implant" is performed ***before*** "forming a silicide on the gate and source/drain regions." As a result, the source/drain extensions of the present invention extend from the isolation trenches 6 to the gate 3, unlike the

lightly doped source and drain regions 30 of Pan which only extend between the oxide layer 26 and the gate 16 of Pan.

In addition, Claim 10 comprises the same sequence of relevant steps as recited in Claim 1. As such, the Applicant respectfully submits the same arguments advanced, supra, to the rejection of Claim 10. Specifically, the step of "performing a vertical source/drain extension implant" is performed before "performing epitaxy to form raised source/drain regions." As a result, the source/drain extensions of the present invention extend from the isolation trenches 6 to the gate 3, unlike the lightly doped source and drain regions 30 of Pan which only extend between the oxide layer 26 and the gate 16 of Pan.

Thus, all the independent claims (i.e., Claims 1, 5, and 10) include a limitation that the source/drain junctions 11 are formed ***before*** the raised source/drain regions are formed; and, as such, the source/drain junctions 11 extend from the isolation trenches 6 to the gate 3 (Fig. 1). Consequently, the Applicant respectfully submits that *the presently claimed forming of the source/drain junctions 11 could not be formed by the method disclosed by Pan, even in view of Wu.*

The Applicant further respectfully submits that the lightly doped source and drain regions 30 are essential to Pan, even in view of Wu. The first sentence of the abstract of Pan focuses on the LLD structure: "A method for forming an LDD structure using a self-aligned halo process is described." As discussed, supra, the method of Pan with respect to the lightly doped (LLD) regions being the goal cannot result in the presently claimed forming of the source/drain junctions 11. In the Summary of the Invention section, Pan teaches (col. 1, ll. 45-54):

> *A principal object of the present invention is to provide an effective and very manufacturable method of forming an LDD structure.*
>
> *A further object of the invention is to provide a method of forming an LDD structure having reduced short channel effects while not increasing junction capacitance.*
>
> *Yet another object is to provide a method of forming an LDD structure using halos having reduced short channel effects while not increasing junction capacitance.* [Emphasis added.]

Consequently, Pan clearly specifies that the LDD is the essential feature and that the halo is secondary feature to the LDD. **Pan does not teach forming the halo independent of the LDD.**

Further, Pan describes a halo in a small critical region relative to the LLD (col. 1, ll. 35-38): "*It is desirable to provide a process to form a halo only in the small critical region.*" [Emphasis added.] Comparing Figure 11 of Pan with Figure 5 of the present application, the halo of Pan is clearly horizontally limited to the region of the LDD and electrically cooperates with the LDD. In contrast, the halo of the present invention substantially overlaps the source and drain junctions 11. Since the LDD is an essential element of Pan, the Applicant respectfully submits that Pan, even in view of Wu, doe not teach, suggest, nor motivate the presently claimed step of forming of the source/drain junctions 11 in combination with the presently claimed step of forming the halo.

CONCLUSION

Accordingly, the pending claims have not been herein further amended and the Applicant believes that the claims have been allowable as originally filed. The Applicant respectfully submits that the presently claimed invention is patentably distinct over the cited references. In view of the foregoing arguments, favorable consideration by the Examiner, withdrawal of the present rejections, allowance of the pending claims, and passage of the present application to issuance are accordingly solicited. ***The Examiner is cordially invited to telephone the undersigned for any reason which would advance the pending claims toward allowance.***

Respectfully submitted,

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